IN THE CLAIMS

1. (original) An electronic silicon device comprising:

a silicon substrate comprising a planar surface;

a trench disposed in said planar surface of said silicon substrate, said trench comprising a wall and a bottom;

a silicon dioxide layer disposed on the bottom of said trench and also on a portion of said wall, said layer being terminated at a distance D below said planar surface of said silicon device;

a polysilicon fill disposed on the surface of said silicon dioxide layer and on a portion of said wall.

2. (original) The electronic silicon device of Claim 1, wherein said polysilicon fill comprises an upper surface that is disposed within a distance D from said planar surface of said silicon substrate.

3. (original) The electronic silicon device of Claim 1, further comprising a junction field effect transistor (JFET).

4. (original) The electronic silicon device of Claim 1, further comprising a metal oxide semiconductor field effect transistor (MOSFET).

5. (original) The electronic silicon device of Claim 1, further comprising an integrated circuit.

6. (original) The electronic silicon device of Claim 1, wherein said trench is disposed above a gate.

7. (original) The electronic silicon device of Claim 1, wherein said trench is disposed adjacent to a source.

8. (original) The electronic silicon device of Claim 1, wherein said silicon dioxide layer is between 100 angstroms and 3000 angstroms in thickness.

9. (original) The electronic silicon device of Claim 1, wherein said silicon dioxide layer is thermally grown.

10. (original) The electronic silicon device of Claim 1, wherein said silicon dioxide layer is deposited.

(Original Claims 11-20 of the Prior Application are canceled herein.)

21. (new) A semiconductor device comprising:

a silicon substrate;

a trench disposed in said silicon substrate, said trench comprising a wall and a bottom;

a silicon dioxide layer disposed on the bottom of said trench and also on a portion of said wall, said layer being terminated below an original surface of said silicon substrate;

a polysilicon fill disposed on the surface of said silicon dioxide layer and on a portion of said wall.

22. (new) The semiconductor device of Claim 21, wherein said polysilicon fill comprises an upper surface that is disposed between a top surface of said silicon dioxide layer and said original surface of said silicon substrate.

23. (new) The semiconductor device of Claim 21, further comprising a junction field effect transistor (JFET).

24. (new) The semiconductor device of Claim 21, further comprising a metal oxide semiconductor field effect transistor (MOSFET).

25. (new) The semiconductor device of Claim 21, further comprising an integrated circuit.

26. (new) The semiconductor device of Claim 21, wherein said trench is disposed above a gate structure.

27. (new) The semiconductor device of Claim 21, wherein said trench is disposed adjacent to a source structure.

28. (new) The semiconductor device of Claim 21, wherein said silicon dioxide layer is between 100 angstroms and 3000 angstroms in thickness.

29. (new) The semiconductor device of Claim 21, wherein said silicon dioxide layer is thermally grown.

30. (new) The semiconductor device of Claim 21, wherein said silicon dioxide layer is deposited.

CONCLUSION

Claims 1-10 and 21-30 remain pending in the present Divisional Application. Claims 11-20 are canceled herein. Claims 21-30 are newly added. Applicant notes that no new matter has been introduced as a result of the amendments presented herein. Applicant respectfully requests that this preliminary amendment be entered into the Divisional Application prior to examination thereof.

The Examiner is invited to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application.

Respectfully submitted,

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